INFORMATION DISCLOSURE STATEMENT BY APPLICANTS PTO-1449	Attorney Docket No. 2885/96	Serial No. 10/551,891
	Applicant(s) VORBACH	
	Filing Date August 28, 2006	Group Art Unit 2183

U.S. PATENT DOCUMENTS

EXAMINER'S INITIALS	PATENT/ PUBLICATION NUMBER	PATENT/PUBLICATION DATE	NAME	CLASS	SUBCLASS	FILING DATE
	4,571,736	February 18, 1986	Agrawal et al.			
	5,477,525	December 19, 1995	Masanobu Okabe			
	5,627,992	May 6, 1997	Baror			
	5,706,482	January 6, 1998	Matsushima et al.			
	5,815,726	September 29, 1998	Cliff			
	5,860,119	January 12, 1999	Dockser			
	6,049,866	April 11, 2000	Earl			
	6,118,724	September 12, 2000	Higginbottom			
	6,188,650	February 13, 2001	Hamada et al.			
	6,247,147	June 12, 2001	Beenstra et al.			
	6,426,649	July 30, 2002	Fu et al.			
	6,483,343	November 19, 2002	Faith et al.			
	6,507,898	January 14, 2003	Gibson et al.			
	6,538,470	March 25, 2003	Langhammer et al.			
	6,598,128	July 22, 2003	Yoshioka et al.			
	6,748,440	June 8, 2004	Lisitsa et al.			
	7,028,107	April 11, 2006	Vorbach et al.			
	7,043,416	May 9, 2006	Lin			
	7,346,644	March 18, 2008	Langhammer et al.			
	7,595,659	September 29, 2009	Vorbach et al.			
	7,650,448	January 19, 2010	Vorbach et al.			
	2001/0003834	June 14, 2001	Shimonishi			
	2002/0156962	October 24, 2002	Chopra et al.			
	2004/0078548	April 22, 2004	Claydon et al.			
	2009/0085603	April 2, 2009	Paul et al.			

FOREIGN PATENT DOCUMENTS

EXAMINER'S INITIALS	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
						YES	NO
	2001-167066	June 22, 2001	Japan			Abstract	
	11-184718	July 9, 1999	Japan			Abstract	
	5-265705	October 15, 1993	Japan			Abstract	

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OTHER DOCUMENTS

EXAMINER'S INITIALS	AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.
	Altera, "APEX 20K Programmable Logic Device Family," Altera Corporation Data Sheet, March 2004, ver. 5.1, pp. 1-117.
	Chaudhry, G.M. et al., "Separated caches and buses for multiprocessor system," Circuits and Systems, 1993; Proceedings of the 36th Midwest Symposium on Detroit, MI, USA, 16-18 August 1993, New York, NY IEEE, 16 August 1993, Pages 1113-1116, XP010119918 ISBN: 0-7803-1760-2.
	Culler, D.E; Singh, J.P., "Parallel Computer Architecture," Pages 434-437, 1999, Morgan Kaufmann, San Francisco, CA USA, XP002477559.
	IMEC, "ADRES multimedia processor & 3MF multimedia platform," Transferable IP, IMEC Technology Description, (Applicant believes the date to be October 2005), 3 pages.
	Jantsch, Axel et al., "Hardware/Software Partitioning and Minimizing Memory Interface Traffic," Electronic System Design Laboratory, Royal Institute of Technology, ESDLab, Electrum 229, S-16440 Kista, Sweden (April 1994), pp. 226-231.
	Kanter, David, "NVIDIA's GT200: Inside a Parallel Processor," http://www.realworldtech.com/page.cfm?ArticleID=RWT090989195242&p=1, September 8, 2008, 27 pages.
	Lange, H. et al., "Memory access schemes for configurable processors," Field-Programmable Logic and Applications, International Workshop, FPL, 27 August 2000, pages 615-625, XP02283963.
	Lee, Ming-Hau et al., "Design and Implementation of the MorphoSys Reconfigurable Computing Processors," The Journal of VLSI Signal Processing, Kluwer Academic Publishers, BO, Vol. 24, No. 2-3, 2 March 2000, pp. 1-29.
	XILINX, "Virtex-E 1.8 V Extended Memory Field Programmable Gate Arrays," (v2.2) September 10, 2002, Xilinx Production Product Specification, pp. 1-52.
	XILINX, "Virtex-II and Virtex-II Pro X FPGA Platform FPGAs: Complete Data Sheet," (v4.6) March 5, 2007, pp. 1-302.
	XILINX, "Virtex-II Platform FPGAs: Complete Data Sheet," (v3.5) November 5, 2007, pp. 1-226.
EXAMINER	DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.